Implementation of Ripple Carry and Carry Look Ahead Adders Using Reversible Logic Gates

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Abstract: Nowadays in the world of VLSI Technology, the word low power consumption is only possible with the concept of Reversible logic design. Reversible concepts will attain more attraction of researchers in the past two decades, mainly due to low-power dissipation and high reliability. It has received great importance due to because of there is no loss of information, while we are processing the data from input to output. Moreover, the power dissipation is also very less and ideally it should be zero. So the concept of reversible design will become more dominant in the low power VLSI design. This paper focuses on the implementation of 4, 8, 16 and 32 bits of highly optimized area efficient Ripple carry adder (RCA) and Carry look ahead (CLA) adders. Finally, we can prove that the Carry look ahead adders are so fastest among all the previously existing designs. All these processes will be Simulated & Synthesized on the ISE Xilinx 14.7 software.

Keywords: Reversible logic, RCA-Ripple Carry Adder, CLA-Carry Look Ahead adders, ISE-Integrated Synthesis Environment, FPGA-Field Programmable Gate Array.

1 INTRODUCTION

Adders. The basic elements in Electronics, which is even more basic elements for implementing the multiplication, division and subtraction. Thus it will be improving the addition speed and improve almost all the arithmetic operations in array processing. Arithmetic and Logical operations, multi operand addition is often encountered. In this way we have a basic adder is ripple carry adder but, there is a one main drawback is, it will take more time to propagate the data from input to Output i.e. delay is more dominant in nature. Due to because of the accumulated delay in ripple carry adders, it can be prohibitively large then we go for carry look ahead adders, with this we are improving the speed of addition and improve the speed of all other

To meet the power and speed design constraints, a variety of methods at different design abstraction levels have been suggested. Approximate computing

Which is an emerging paradigm deals with demand performance and power efficiency constraints for adders at the cost of reducing the computational accuracy of the result [2]. This paradigm is especially suitable for applications where the answer is not unique and a set of approximate answers are acceptable. These applications include multimedia processing, machine learning, signal processing, and other error resilient computations [2]. Approximate arithmetic units are mainly based on the simplification of the arithmetic units circuits. Different structures for approximate adders have been proposed – see for example, [3], [5]-[14]. Most of the proposed adders are fully approximate and may only be utilized in error resilient applications. At the same time, some of these structures have a constant level of deviation from the actual result, i.e., during the system operation their accuracies are not tuneable. Runtime accuracy reconfigurability, however, may be considered as a useful feature for a system providing different levels of quality of service (QoS) during operation [3]-[5]. Here, by reducing the quality, the total computation time and/or power consumption of the unit are reduced resulting in higher energy efficiency. In addition, some digital systems, such as general purpose processors (GPPs), may be utilized for both approximate and exact computing, necessitating the ability to dynamically switch between exact and approximate operating modes. This feature may be obtained by adding a correction unit to the approximate circuit that would turn the approximate solution to an exact solution. The correction unit, however, increases the delay, power and area overhead of the design. Also, the error correction procedure may require more than one Clock cycle (e.g., see, [6],[13]), which could slow down the processing. In this paper, we present a Reconfigurable Approximate Carry Look-Ahead Adder (RAP-CLA) which has two operating modes of exact and approximate. The structure of the adder, which is based on the conventional CLA adder, does not require an external correction unit for the exact add operation. While the delay and power consumption of the proposed adder, in the exact mode, are about the same as those of the conventional CLA, they are considerably smaller in approximate mode. This is because, in the approximate mode by exploiting the power gating technique, the power consumption is significantly reduced.
II GOALS OF REVERSIBLE LOGIC

- **Garbage Output**: The total number of unused outputs present in the design.
- **Number of reversible logic gates**: The total number of reversible gates is used in the circuit.
- **Delay**: The time taken by the propagation of inputs to the output, i.e., the speed of the circuit.
- **Ancillary bits**: The total number of inputs which are maintained either constant 0 or 1 in order to get the proper output.
- **Quantum cost**: The number of 1x1 & 2x2 reversible logic gates or Quantum logic used in the design.

III EXISTING REVERSIBLE LOGIC GATES

A. Feynman Gate
It is a 2x2 Feynman logic gate with the Quantum cost of 1 is shown in fig 1. It is also known as CNOT gate.

![Fig. 1 Feynman gate logic diagram](image1)

![Fig. 2 Quantum implementation of Feynman gate](image2)

![Figure:3 Double Feynman gate logic diagram](image3)

B. Double Feynman Gate
It is a 3x3 Feynman gate with the Quantum cost of 2 is shown in fig 3.

![Figure 4: Quantum implementation of Double Feynman gate](image4)

C. Peres Gate
It is a 3x3 Peres logic gate with the Quantum cost of 4 is shown in fig 5.

![Figure 5: Peres gate logic diagram.](image5)
They proposed a two-qubit quantum entryway library that assumes a noteworthy part in decreasing GHz operation with a 5 cycle latency. The designs have been fabricated using the 2.5kA/cm$^2$ AIST standard process and have demonstrated successful operation in low-frequency testing. Both adders consist of $\sim$1000 Josephson junctions and are designed for 5 GHz operation with a 5 cycle latency.

V LITERATURE SURVEY

L. Ayala, Member, IEEE, Naoki Takeuchi, et.al. Superconductor-based adiabatic quantum-flux parameter on (AQFP) logic holds tremendous promise towards building extremely energy efficient computing systems with bit energies approaching 100 $k_B T$. The majority logic gate is the basis for how all AQFP logic gates are created. By reconsidering the logic design approach of digital circuits using majority logic instead of conventional AND/OR/NOT logic, circuits can potentially use fewer gates overall. This may lead to lower circuit complexities in terms of Josephson junctions, and in turn lower power consumption as well as lower latencies. As a first step towards exploiting majority logic in AQFP technology, we explore how majority-logic-optimized designs of the Kogge-Stone and Brent-Kung adder architectures scale in terms of complexity, latency, area and energy/operation as we increase the data word size from 8-bit to 64-bit. Next, we implement 8-bit prototypes of both adders for experimental demonstration. The designs have been fabricated using the 2.5kA/cm$^2$ AIST standard process and have demonstrated successful operation in low-frequency testing. Both adders consist of $\sim$1000 Josephson junctions and are designed for 5 GHz operation with a 5 cycle latency.

Omid Akbari1, Mehdi Kamal et.al. In this paper, we propose a fast yet energy-efficient reconfigurable approximate carry look-ahead adder (RAP-CLA). This adder has the ability of switching between the approximate and exact operating modes making it suitable for both error resilient and exact applications. The structure, which is more area and power efficient than state-of-the-art reconfigurable approximate adders, is achieved by some modifications to the conventional carry look ahead adder (CLA). The efficacy of the proposed RAP-CLA adder is evaluated by comparing its characteristics to those of two state-of-the-art reconfigurable approximate Adders as well as the conventional (exact) CLA in a 15nm Fin FET technology. The results reveal that, in the approximate operating mode, the proposed 32-bit adder provides up to 55% and 28% delay and power reductions compared to those of the exact CLA, respectively, at the cost of up to 35.16% error rate. It also provides up to 49% and 19% lower delay and power consumption, respectively, compared to other approximate adders considered in this work. Finally, the effectiveness of the proposed adder on two image processing applications of smoothing and sharpening is demonstrated. The study shows that, on average, PSNR reductions of 12% and 16%, respectively, may be achieved by employing the proposed adder.

In 2015, C.H. BENNETT depicted that if a calculation is done in Reversible rationale zero vitality dissemination is conceivable, as the measure of vitality scattered in a framework is specifically identified with the quantity of bits eradicated amid calculation. The outline that does not bring about data misfortune is irreversible. Arrangements of reversible gates are expected to plan reversible circuit. Reversible gate can produce remarkable output vector from every input vector and the other way around [2].

In 2008, Majid Mohammdi et.al exhibited those quantum gates to execute the parallel reversible rationale gates. Quantum gates V and V+ to be spoken to in truth table structures. Creator Demonstrated that few reversible circuit benchmarks are enhanced and contrast and existing work. Another behavioral model to speak to the V and V+ quantum gates based on their properties. This model used to recreate the quantum realization of reversible circuits [3]. In 2010, D.Michael Mill operator and Zahra Sasanian exhibited the lessening the quantity of quantum gate expense of reversible circuits. To diminish the quantum cost enhances the proficiency of the circuit. To decide a quantum circuit is to first union circuits made out of parallel reversible gates then guide that circuit to a proportional quantum gate.

Acknowledgment [4] CMOS, Quantum PC, Nanotechnology, Optical registering and self-repair [5]. In 2011, Md.Mazder Rahman et.al displayed a quantum gate library that comprises of all conceivable two-Qubit Quantum gates which Don’t produce trapped states. These gates are utilized to decrease the quantum cost of reversible circuits. They proposed a two-qubit quantum entryway library that assumes a noteworthy part in decreasing...
the quantum expense of reversible gates [6]. In 2012, B.Raghu Kanth et.al depicted that actualizing of reversible circuit reducing garbage outputs, gate count and constant inputs, gates tally and consistent inputs. Expansion, Subtractions operations are acknowledged utilizing reversible DKG gate and it contrast and ordinary doors. The proposed reversible adder/subtractor circuit can be connected to outline of complex frameworks in nanotechnology [7].

In 2012, Mr. Devendra Goyal exhibited VHDL CODE of all Reversible Rationale Entryway, which give us to plan VHDL CODE of any complex successive circuit. Here creator have been attempted to make the VHDL code however much as could reasonably be expected. Creator can reenact and combination it utilizing Xilinx programming [8]. In 2013, Marek Szyprowski exhibited a device for minimizing the quantum cost in 4-bit reversible circuits. Here Creator demonstrated that for benchmarks and for plans taken from late distributions it is conceivable to acquire sparing in quantum cost contrasting and existing circuits [9]. In 2013, Raghava Garipelly gave that the essential reversible logic gates, which in planning of more intricate framework having reversible circuits as a primitive segment and this can execute more convoluted operations utilizing quantum computers. Creator presented some new gates which are BSCL, SBV, NCG, and PTR and so forth [10].

In 2014, Ashima Malhotra et.al portrayed that reversible adjusted Fredkin entryway used to plan the multiplexers with low quantum cost and contrast it and existing work. They likewise look at the quantum expense of multiplexers outline utilizing, Fredkin door with Changed Fredkin gate used to plan the multiplexers [11].

Table I: Truth table for full adder using peres gate

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VI PROPOSED DESIGNS

A. Ripple Carry Adder :

To designing the Ripple carry adder, the basic element is full adder. So firstly we can design a modified reversible full adder for getting the optimized results by using simple 3*3 Peres gate [10] only is shown in the fig 5. It is proved that the modified reversible full adder design can be realized with two garbage outputs and only on ancillary input. While we are designing the full adder, the 3rd input of the first Peres gate should be considered as zero. The output of the ripple carry adder is shown below.

Sum = \( A \oplus B \oplus C \)

\[ \text{Carry} = (A \oplus B). \text{Cin} \oplus AB \]

Figure 9 Full adder design using Peres gate.

RCA requires n-bit full adder design circuits, ripple carry adder propagates their individual carry input through each and every full adder circuit blocks. The output carry of the \( i \)th full adder circuit is connected to \( (i+1) \)th full adder design circuit. Thus the coming next full adder circuit has to wait until the previous logic block to provide the carry for particular stage. Finally, it will provide the sum and carry afterwards the \( n \)-stages for \( n \)-bit RCA addition. The output of the first Peres gate is applied to the inputs of the second Peres gates respectively. Hence the sum and carry are generated at the final stages of the ripple carry design.
This paper proposed the architecture for 4-bits of ripple carry adder only, but we can synthesize, simulate and FPGA implementation of remaining 8, 16, 32 bit ripple carry adders also. In this way it is possible to design any bit ($n^{th}$) of Ripple carry addition also. The simulation result of 32-bit ripple carry adder is shown in fig 13.

B. Carry Look Ahead Adder

Here we are designing basic elements of NFT [4] gate and Double Feynman gate for designing of CLA. The main purpose of selecting the NFT gate is that it preserving the parity bits, if there are no faults occurred in the signal level, then there is no need of requirement of intermediate signals. In this paper, we proposed a design and implementation of 32-bit CLA that is efficient in terms of delay, apart from these we

VII CONCLUSION

In this paper, we proposed the area efficient Ripple carry adder and Carry look ahead adder. The realization of the RCA CLA is designed by using the basic full adder circuit, this can be realized by Using two basic Peres gates only, that is the reason why only we can design these adders having less delay with comparison to the almost all the previous existing be used furthermore has played a very crucial role in future development of Quantum computers.

Whatever the design we are proposed in this paper, by using parity. The basic purpose of the addition using CLA is to generate all incoming carries in parallel and to avoid the waiting until the propagation of carries from the previous stages of full adder. used in CLA are parity preserving gates. Hence the whole design of adder preserves the that all the reversible logic gates will be preserved for parity bits, but both logic gates are designing 4,8,16 bits of CLA also and it can be simulated and compare the results of delay with the existing designs. There is no possibility this it is possible to design any bit ($n^{th}$) of designing in RCA and CLA by simply cascading of each and every individual designs. Finally, we proposed an Ultra speed implementation of RCA and CLA. designs. It can be proved by comparing our proposed Design to the existing design is shown in the above table.
Complexity of the circuit, this is providing a good environment for speed processing environments, not only the parameter of delay, we can put a more concentration on the Quantum cost [1] and Power dissipation. In the world of low power VLSI design everything is possible, might be in the future the full adder design is more precise than all the previous existing designs, then we may get the more ultra speed adders are designed well, it helps to design RCA and CLA are more optimized, so it is also very much needful in Quantum computing. Till now all the research work is done on reversible logic gates.

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